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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,057	05/30/2000	Dale E Parson	3-2-1-4	1195

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	PAPER NUMBER
2184	7

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

7

Office Action Summary	Application No.	Applicant(s)	
	09/583,057	PARSON ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

- **Claims 1, 10, 11, 13, 14, 19, and 20 are rejected by Spix, et al, U.S. Patent Number 5,253,359 and Jaber, U.S. Patent Number 6,028,983.**
- **Claims 2 and 3 are rejected by Spix, Jaber, and Moiin, U.S. Patent Number 6,108,699.**
- **Claims 4, 5, 8, 12, 15, 16, 17, 18, are rejected by Spix, Jaber, and Cromer, U.S. Patent Number 6,263,373.**
- **Claims 6-7 are rejected by Spix, Jaber, Moiin, and Cromer.**

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 10, 11, 13, 14, 19, and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Spix, et al, U.S. Patent Number 5,253,359, and further in view of Jaber, U.S. Patent Number 6,028,983. Regarding claim 1, and further regarding the limitation of defining a subset of processors, Spix discloses a system that has the ability to access, control, set and sense processes over a highly parallel multiprocessor system. (Lines 34-38 of Column 1 and Lines 27-31 of Column 4). Regarding the limitation of delaying issuance of commands, Spix discloses that a scan path allows processors to be initialized and then the controller senses machine states in the group. In Figure 6, there are steps that are in between the initialization (block 208) and

controller sensing machine states (block 212). Processor maintenance is performed once machine state is sensed. (See Figure 6, Items 208, 210, 212, 214, 216, 220, and Lines 38-65 of Column 10). Spix does not disclose the use of a group scan command. Jaber discloses a system with means of using a JTAG port to scan microprocessor chips. (Lines 54-56 of Column 3 and Lines 6-7 and 16-22 of Column 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix discloses that it would be useful for setting and sensing capability in a highly parallel processing system. (Lines 22-27 of Column 3).

3. Regarding claim 10, Spix discloses a system that can be comprised of workstations or other computer and storage devices. (Lines 37-47 of Column 3).

4. Regarding claim 11, Spix discloses a system that provides control and maintenance of a multiple processor system. (Lines 22-25 of Column 4).

5. Regarding claim 13, Spix discloses that a scan path allows processors to be initialized and then the controller senses machine states in the group. Processor maintenance is performed once machine state is sensed. (See Figure 6, Items 208, 210, 212, 214, 216, 220, and Lines 38-65 of Column 10). Spix does not disclose the use of a group scan command. Jaber discloses a system with means of using a JTAG port to scan microprocessor chips. (Lines 54-56 of Column 3 and Lines 6-7 and 16-22 of Column 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix discloses that it would be useful for setting and sensing capability in a highly parallel processing system. (Lines 22-27 of Column 3).

6. Regarding claim 14, Spix discloses that maintenance software comprises a portion of the system. (Lines 10-21 of Column 4).

7. Regarding claim 19 and further regarding the limitation of defining a subset of processors, Spix discloses a system that has the ability to access, control, set and sense processes over a highly parallel multiprocessor system. (Lines 34-38 of Column 1 and Lines 27-31 of Column 4). Regarding the limitation of delaying issuance of commands, Spix discloses that a scan path allows processors to be initialized and then the controller senses machine states in the group. Processor maintenance is performed once machine state is sensed. (See Figure 6, Items 208, 210, 212, 214, 216, 220, and Lines 38-65 of Column 10). Regarding the limitation of receiving a command from one or more processors, Spix discloses system that can receive commands from processing units for setting and sensing diagnostic problems. (Lines 65-68 of Column 1 and 1-2 of Column 2). Spix does not disclose the use of a group scan command. Jaber discloses a system with means of using a JTAG port to scan microprocessor chips. (Lines 54-56 of Column 3 and Lines 6-7 and 16-22 of Column 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix discloses that it would be useful for setting and sensing capability in a highly parallel processing system. (Lines 22-27 of Column 3).

8. Regarding claim 20, Spix discloses that a scan path allows processors to be initialized and then the controller senses machine states in the group. Processor maintenance is performed once machine state is sensed. (See Figure 6, Items 208, 210, 212, 214, 216, 220, and Lines 38-65 of Column 10). Spix does not disclose the use of a group scan command. Jaber discloses a system with means of using a JTAG port to scan microprocessor chips. (Lines 54-56 of Column

3 and Lines 6-7 and 16-22 of Column 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix discloses that it would be useful for setting and sensing capability in a highly parallel processing system. (Lines 22-27 of Column 3).

9. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spix and Jaber as applied to claim1 above, and further in view of Moiin, U.S. Patent Number 6,108,699. Regarding claim 2, Spix discloses a system that can define a subset of processors and delay issuance of a command until a scan command is received. Spix does not disclose a system that contains the ability to define a group of processors. Moiin disclose a system that can define a group of processors by petitioning member nodes for reconfiguration. (Lines 10-20 of Column 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the reconfiguration of member processors to the system of Spix so that defective processor might be removed from the system. (Lines 7-13 of Column 1 of Spix).

10. Regarding claim 3, Moiin discloses a system that can store information about group member states. (Lines 55-65 of Column 8 and Figure 3 and 5 steps 308 and 508).

11. Claims 4-5, 8, 12, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spix and Jaber as applied to claim1 above, and further in view of Cromer, U.S. Patent Number, 5,253,359. Regarding claim 4, Spix discloses a system that can define a subset of processors and delay issuance of a command until a scan command is received. Spix does not teach that these commands are configured in accordance with IEEE 1149.1 standard. Cromer teaches that an IEEE1149.1 standard can be used to debug and test processors. (Lines 59-62 of Column 1). It would have been obvious to one of ordinary skill in the art at the time of the

invention to use the IEEE1149.1 standard for debug and testing to issue commands for debug and testing.

12. Regarding claim 5, Spix discloses a system that can define a subset of processors and delay issuance of a command until a scan command is received. Spix does not teach that these commands are configured in accordance with IEEE 1149.1 standard. Cromer teaches that a test access port (TAP) can be used to debug and test processors. (Lines 59-62 of Column 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the test access port (TAP) for debug and testing to issue commands for debug and testing.

13. Regarding claim 8, Spix discloses a system that can define a subset of processors and delay issuance of a command until a scan command is received. Spix does not teach that these processors are homogenous processors. Cromer teaches that a test access port (TAP) can be used to debug and test processors that are found in all Pentium™ class processors. (Lines 59-62 of Column 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a Pentium™ class processors so that a TAP and IEEE standard 1149.1 would be incorporated into the processor. (Lines 63-68 of Column 1 and 1-20 of Column 2 of Cromer).

14. Regarding claim 12, Spix does not teach the uses of single serial bit stream to communicate commands with the processors. Cromer teaches the uses of a serial bit stream for communications. (Lines 50-58 of Column 5). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a serial bit stream in to the system of Spix so that the processors could communicate with each other. Both Spix (Lines 40-43 of Column 3) and Cromer (Lines 58-63 of Column 3) use Ethernet net for communication between processors, so it would have been advantageous to use a common communications stream.

15. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cromer, et al, U.S. Patent Number 6,263,373, and further in view of Spix, et al, U.S. Patent Number 5,253,359 and Jaber, U.S. Patent Number 6,028,983. Regarding claim 15 and further regarding the limitation of a debugger, Cromer discloses a system that uses a TAP for debugging. (Lines 23-25 of Column 2). Regarding the limitation on a scheduler coupled to the debugger, Cromer discloses a system that has a special purpose processor for receiving signals from client computers for determining debug commands. (Lines 30-37 of Column 3). Regarding the limitation of a generator for generating test commands, Cromer discloses a system that has a special purpose processor that has the ability to generator debug commands. (Lines 37-45 of Column 3). Cromer does not teach the use of a chain manager to delay issuance of commands. Spix discloses that a scan path allows processors to be initialized and then the controller senses machine states in the group. Processor maintenance is performed once machine state is sensed. (See Figure 6, Items 208, 210, 212, 214, 216, 220, and Lines 38-65 of Column 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the scan path of Spix into the system as disclosed by Cromer because it would have been advantageous to have a system to set and sense client processor states, and it would have been advantageous to have a system able to set and sense states after the response of a signal from the client. (Lines 54-59 of Column 3 of Spix, and Lines 29-34 of Column 2 of Cromer). Spix does not disclose the use of a group scan command. Jaber discloses a system with means of using a JTAG port to scan microprocessor chips. (Lines 54-56 of Column 3 and Lines 6-7 and 16-22 of Column 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix

discloses that it would be useful for setting and sensing capability in a highly parallel processing system. (Lines 22-27 of Column 3).

16. Regarding claim 16, Cromer discloses a system that has test generators for producing test for each processor. (Lines 30-45 of Column 3).

17. Regarding claim 17, Cromer discloses a system that has a scan that is received and sent as a serial bit stream. (Lines 50-58 of Column 5).

18. Regarding claim 18, Spix discloses a system that has a maintenance system that is disposed partly in software. (Lines 10-22 of Column 4).

19. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spix and Jaber as applied to claim1 above, and further in view of Cromer, U.S. Patent Number, 5,253,359 and Moiin, U.S. Patent Number 6,108,699. Regarding claim 6, in view of Spix and Cromer, Spix and Cromer do not show TAP managers/process being in a signal cluster of processors. Moiin shows a cluster of computers and talks of a processor leaving a group of computers and entering a group of clusters. An identifying field is set in the processor to identify which process group the processor belongs to. Thereby, a processor can only belong to one group at one time. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the cluster ability of Moiin with the system of Spix and Cromer so that the system could easily determine which cluster the processor is in.

20. Regarding claim 7, in view of Spix and Cromer, Spix and Cromer do not show TAP managers/process being in a signal cluster of processors. Moiin, U.S. Patent Number 6,108,699 shows a cluster of computers and talks of a processor leaving a group of computers and entering a group of clusters. An identifying field is set in the processor to identify which process group

the processor belongs to. Thereby, a processor can only belong to one group at one time. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the cluster ability of Moiin with the system of Spix and Cromer so that the system could easily determine which cluster the processor is in.

Response to Arguments

21. Regarding the status of claims 6 and 7. The examiner would like to apologize for any misunderstanding. Claims 6 and 7 are rejected (as stated above) and are **NOT** in condition for allowance. Claims 1-20 were rejected in previous action, paper number 5.

22. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. See above rejects. The examiner would like to make the following response to applicant's arguments.

23. The applicant argues against the examiner's rejections based on 102a (Lines 7 of page 3 of pager 6). These arguments have zero bases because the examiner made no such rejections in the non-final office action (paper number 5). The examiner believes that "102a" was an error in typing and should be read as 102b.

24. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.** The examiner can normally be reached on **Mon-Fri: 7:30-5:00, every other Friday off**. The examiner can be reached at: **703-305-7762**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Rob Beausoliel** can be reached on **703-305-9713**. The fax phone numbers for the organization where this application or proceeding is assigned are:

703-746-7239 for regular communications

703-746-7240 for After Final communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **703-305-3900**.

Responses should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC 20231

NADEEM IQBAL
PRIMARY EXAMINER

Tim Bonura
Examiner
Art Unit 2184

tmb
September 4, 2003